REMARKS

Claim Rejections 35 U.S.C. § 102 (a)

The Examiner has rejected claims 8 and 10 – 14 under 35 U.S.C. §102 (a) as being anticipated by Matsumoto et al. (US 5,726,479, of record) or Chen (US 5,290,720, of record).

It is the Examiner's position that Matsumoto et al. discloses a gate electrode formed on a substrate comprising,

a gate layer (4) disposed above a substrate (1);

thin first spacers (5) disposed adjacent to opposite sides of the gate layer wherein tops of the thin first spacers are at approximately the same height as a portion of top of the gate layer;

thick second spacers (36) disposed adjacent to each of the thin first spacers, the thick second spacers having a flat upper surface, wherein tops of the thick second spacers are at approximately the saem height as a portion of top of the gate layer;

a conductive layer (9a) disposed on the gate layer, the conductive layer extending beyond edges of the gate layer;

wherein the gate layer comprises polysilicon;

wherein the conductive layer comprises polycide;

wherein the thin first spacers comprise oxide;

wherein the thick second spacers comprise nitride;

wherein the polycide comprises titanium salicide ($TiSi_2$).

It is further the Examiner's position that Chen also teaches a gate electrode identical to the claimed gate structure.

Applicant respectfully disagrees. The gate electrode of Applicant's claim 8, as amended, is not anticipated by either of the two references cited by the Examiner: Matsumoto et al. or Chen.

In the gate electrode of Applicant's claimed invention, such as shown in Figure 3I, both the thin first spacers (330) and the thick second spacers (340) have approximately the same height as the gate layer (320). However, in the gate electrode of the cited reference of Matsumoto et al., both the thin first spacers (5) and the thick second spacers ((7a) have much lower heights than the gate layer (4a). See Figures 8 – 10 (f) and Figures 18 – 21 (e) of Matsumoto et al.

Additionally, in the gate electrode of Applicant's claimed invention, such as shown in Figures 3C – 3I, the thick second spacers (340) comprise nitride. However, in the gate electrode of the cited reference of Chen, the thick second spacers (23) comprise Silicon. See Figure 4 and Col. 3, line 41 of Chen.

Furthermore, the gate electrodes of Applicant's claims 10 – 12 and 14 are also not anticipated by Matsumoto et al. or Chen since claims 10 – 12 and 14 are dependent on claim 8, as amended.

Claim 13 has been canceled without prejudice.

Consequently, neither Matsumoto et al. nor Chen, teaches each and every element of Applicant's claimed invention. In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections under 35 U.S.C. §102 (a) to claim 8, as amended, and claims 10 – 12 and 14.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

8. (Twice Amended) A gate electrode comprising:

a gate layer disposed above a substrate;

thin first spacers disposed adjacent to opposite sides of said gate layer wherein [tops of] said thin first spacers have [are at] approximately the same height as [top of] said gate layer;

thick second spacers disposed adjacent to each of said thin first spacers, said thick second spacers comprising nitride [said thick second spacers having a flat upper surface], wherein [tops of] said thick second spacers have [are at] approximately the same height as [top of] said gate layer; and

a conductive layer disposed over [on]